REMARKS

By this response, claims 1-17 are pending, of which claims 1, 4, 11 and 14 are amended. No new matter has been introduced. Adequate descriptive support for the amendment can be found in, for example, Fig. 5; page 17, lines 2-6; and page 22, lines 21-29.

The Office Action dated June 5, 2002 allowed claims 11-13, and rejected claims 1, 4 and 14 under 35 U.S.C. §102(b) as being anticipated by Hsu (U.S. Patent No. 5,805,003). Claims 2, 3, 5-10 and 15-17 were objected to, but would be allowable if rewritten in independent form. The rejection and objection are respectfully traversed in light of the remarks presented herein.

THE ANTICIPATION REJECTION OF CLAIMS 1, 4 AND 14 IS TRAVERSED

Claims 1, 4 and 14 were rejected as being anticipated by Hsu. The rejection is respectfully traversed because Hsu cannot support a prima facie case of anticipation.

A *prima facie* case of anticipation under 35 U.S.C. § 102 requires that a single prior art reference must disclose each and every element as set forth in the subject claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Hsu does not meet these requirements.

Although Hsu's circuit includes a delay circuit, a phase detector, and gray code counters, the interconnections between the components, the operations, and signal flows are different from those required by the claims. For example, claim 1, as amended, recites

"A delay locked loop comprising: a delay circuit...; a detector detecting which of said first and second clocks is advanced in a phase; and a gray code counter using a gray code, responsive to an output of said detector for generating a signal to increase or decrease an amount of delay of said delay circuit."

In contrast, according to Hsu, the output (Fout) of the gray code counter 16 does not increase or decrease an amount of delay of the delay circuit, as required by claim 1. Furthermore, Hsu's phase detector output directly feeds to a loop filter 46, and is not used to control the operations of the gray code counters. Thus, Hsu's gray code counters do not generate a signal in response to an output of the phase detector. Accordingly, Hsu fails to disclose every limitation of claim 1, the anticipation rejection is untenable and should be withdrawn. Favorable consideration of the claim is respectfully requested.

Claims 4 and 14 are also rejected as being anticipated by Hsu. Claim 4, as amended, is directed to a semiconductor device having a structure similar to that of claim 1, and claim 14, as amended, is a method claim that has claim scope comparable to that of claim 1. Thus, the anticipation rejection of claims 4 and 14 is also untenable and should be withdrawn based on at least the same reasons discussed in claim 1 as well as on their own merits.

CONCLUSION

Therefore, the present application claims subject matter patentable over the references of record and is in condition for allowance. Favorable consideration is respectfully requested. If there are any outstanding issues that might be resolved by an

interview or an Examiner's amendment, Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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Recognition Under 37 C.F.R. §10.9(b)

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VERSION WITH MARKINGS SHOWING CHANGES MADE

IN THE CLAIMS:

Please amend the following claims:

1. (Amended) A delay locked loop comprising:

a delay circuit delaying a first clock to output a second clock;

a detector detecting which of said first and second clocks is advanced in a phase [difference between said first and second clocks]; and

a gray code counter using a gray code, responsive to an output of said detector for generating a signal [adjusting] to increase or decrease an amount of delay of said delay circuit.

4. (Amended) A semiconductor device comprising a delay locked loop including:

an input buffer receiving an external clock and outputting a first internal clock;

a delay circuit delaying said first internal clock to output a second internal clock;

a detector detecting which of said first and second clocks is advanced in a phase [difference between said first and second internal clocks]; and

a gray code counter using a gray code, responsive to an output of said detector for generating a signal [adjusting] to increase or decrease an amount of delay of said delay circuit.

11. (Amended) A semiconductor device comprising a delay locked loop including:

a first input buffer receiving at least a first external clock and a second external clock complementary in phase to said first external clock, and outputting a first internal clock at the timing of the rising edge of said first external clock when a potential of said first external clock is equal to that of said second external clock;

a second input buffer receiving at least said first and second external clocks, and outputting a second internal clock at the timing of the rising edge of said second external

clock when a potential of said first external clock is equal to that of said second external clock;

a first delay circuit delaying said first internal clock to output a third internal clock;

a second delay circuit delaying said second internal clock to output a fourth internal clock;

a detector detecting which of said first and second clocks is advanced in a phase [difference between said first and third internal clocks]; and

a gray code counter using a gray code, responsive to an output of said detector for generating a signal [adjusting] to increase or decrease an amount of delay of said first delay circuit and an amount of delay of said second delay circuit.

14. (Amended) A control method for a system operating in synchronization with a clock, comprising the steps of:

inputting an external clock to an input buffer to generate a first internal clock therefrom;

delaying said first internal clock to output a second internal clock;

detecting which of said first and second clocks is advanced in a phase [difference between said first and second internal clocks]; and

using a gray code to [determine] increase or decrease an amount of delay to be applied in the step of delaying, said amount of delay corresponding to a result obtained in the step of detecting.